Abstract

An apparatus permits built-in self-test ("BIST") of an IC that includes a memory element having one or more impermissible operations. A code generator accepts a clock signal and generates a test code in response to it. A decoder accepts the test code and generates at least two output lines where when in a decode enabled condition, the output lines are responsive to the test code and reflect a value that is combined with respective memory access lines comprising first and second write address outputs and first and second read address outputs as well as enable bits from first and second write enable registers and first and second read enable registers to disable the one or more impermissible operations. When the decoder is in a decode disabled condition, the output lines reflect a value that when combined with the respective memory access lines enables all possible memory operations.

The teachings also include a method for BIST of an IC including a memory element having one or more impermissible operations having the steps of storing a seed value into a code generator, generating a test code in response to a clock signal, and mapping the test code to at least two output lines. The steps continue by combining respective ones of the output lines with a memory operation signal to generate a memory access enable signal, where when in a test code enabled condition, the step of mapping causes the output lines to reflect values that when performing the step of combining, the resulting memory access enable signals disable the one or more impermissible operations. Furthermore, when in a test code disabled condition, the step of mapping causes the output lines to reflect values that when performing the step of combining, the resulting

memory access enable signals permit all possible memory operations without intervention.